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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,195	07/16/2001	Nobuaki Shinmori	KAN 135	3051

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EXAMINER	
DAMIANO, ANNE L	

ART UNIT	PAPER NUMBER
2114	5

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/905,195	SHINMORI
	Examiner	Art Unit
	Anne L Damiano	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 2 recites the limitation "the inverted level of the one of the Pin scramble-circuit output" in lines 6-7. There is insufficient antecedent basis for this limitation in the claim. Other limitations: namely "the security bit" of line 2, "the JTAG control circuit" of line 3, "the output of the security bit" of line 8 also lack antecedent basis.

5. Claim 3 recites the limitation "the inverted level of the one of the debug enable register output" in lines 6-7. There is insufficient antecedent basis for this limitation in the claim. Other

limitations: namely "the security bit" of line 3, "the JTAG control circuit" of line 4, "the output of the security bit" of line 8 also lack antecedent basis.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 4-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (6,662,314).

As in claim 1, Iwata discloses a semiconductor circuit wherein a JTAG control circuit (Figure 2: component 15) controlled by the security bit of a flash ROM (figure 1: component 5 and column 4: line 64-column 5: line 6)) is equipped between the JTAG port (interface terminals-figure 2: component 11) and a TAP (Test Access Port) (figure 2 components 15 and column 5: lines 63-column 6: lines 3). (The JTAG port and TAP are encompassed in the JTAG controller. Therefore, the JTAG control circuit is between the JTAG port and the TAP.)

As in claim 4, Iwata discloses a semiconductor circuit having a security releasing means comparing the data which is input a test port with the data stored in a memory device (debug-related control register) and turning on a switch when the two data agree (column 5: line 67-column 6: line 2 and column 6: lines 4-8), (In determining if a condition is satisfied, the input data is compared to the data in the memory device.)

The semiconductor circuit comprising: a memory device to store a control program and data (internal flash) (column 1: lines 6-65);

A central processing unit to execute a specific process according to the program (column 2: lines 41-46 and column 6: lines 5-24);

A test port to input and output test signals (JTAG interface terminals) (column 5: lines 63-66); and

A switch to control on/off (mode) between the test port and the memory device and/or the central processing unit according to the security bit set in a nonvolatile register (column 1: line 64-column 2: line 5 and column 4: line 64-column 5: line 6).

As in claim 5, Iwata discloses the semiconductor circuit according to claim 4 wherein the security releasing means comprising: an address register keeping the address information input from the test port and specifying the memory range of the memory device (column 8: lines 6-9);

A data register keeping the data information input from the test port (column 18: lines 56-58); (The security information input from user must be stored in order for the comparison to be made.)

A comparator comparing the data read out from the memory device based on the address information with the data kept in the data register (column 18: lines 42-61); and

A logic gate turning on a switch when the two data agree, independent of the state of security bit (column 18: line 66-column 19: line 10). (Some form of logic gate must be existent for the different modes to occur.)

As in claim 6, Iwata discloses the semiconductor circuit according to the claim 4 wherein the security releasing means comprising: an address counter counting the timing information input from the test port sequentially and specifying the memory range (column 8: lines 6-9);

A data register keeping the data information input from the test port (column 18: lines 56-58) (The security information input from user must be stored in order for the comparison to be made);

A comparator comparing the data read out from the memory device based on the specification of the address counter with the data kept in the data register (column 18: lines 42-61);

An agreement number counter (byte count) outputting a releasing signal when the number of agreement of the data comes to the specific value (that which exceed 4 bytes) (column 18: lines 52-54); and

A logic gate turning on a switch when the releasing signal is output, independent of the state of security bit (column 18: line 52-column 19: line 10). (When the number counter comes to a specific value, the security codes are re-obtained. Some form of gate must be existent for this mode to occur.)

As in claim 7, Iwata discloses the semiconductor circuit according to claim 6 comprising an address register setting the initial value based on the address information input from the test port (column 15: lines 59-column 16: line 4).

As in claim 8, Iwata discloses a semiconductor circuit comprising: a memory device to store a control program and data;

A central processing unit to execute a specific process according to the program (column 2: lines 41-46 and column 6: lines 5-24);

A test port to input and output test signals (JTAG interface terminals) (column 5: lines 63-66);

A switch to control on/off between the test port and the central processing unit (column 1: line 64-column 2: line 5 and column 4: line 64-column 5: line 6); and

A security releasing means comparing the data input a test port with the data stored in a memory device and turning on a switch when the two data agree (column 18: line 66-column 19: line 10). (Some form of switch must be existent for the different modes to occur according to the outcome of the comparison.).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

SCOTT BADERMAN
PRIMARY EXAMINER